CLAIMS

1. A method comprising:

selecting a row from a plurality of rows in a pixel array;

opening a path between a first line having a first voltage and a bus through one or more row select transistors;

selecting the row for reset;

opening a path between a second line having a second voltage and the bus through one or more reset enable transistors, said second voltage being higher than said first voltage; and

providing the second voltage to the one or more row select transistors.

2. The method of claim 1, wherein the one or more row select transistors comprise PMOS transistors, each including an n-well.

3. The method of claim 2, wherein said providing the second voltage to the one or more row select transistors comprises boosting the n-wells of the PMOS transistors to the second voltage.

4. The method of claim 1, wherein the second voltage comprises a boosted reset voltage.

5. A row driver comprising:

a bus;

a first line operative to carry a select voltage;

a second line operative to be driven to a boosted voltage, said boosted voltage being higher than the select voltage;

a first circuit operative to couple the bus to the first line in response to a row select signal, said first circuit including a transistor coupled to the second line.

6. The row driver of claim 5, further comprising a second circuit operative to couple the bus to the second line in response to a row reset signal.

7. The row driver of claim 5, wherein the transistor is coupled to the second line such that there is no parasitic diode leakage between the first line and the second line through the transistor in response to the second line being driven to the boosted voltage.

8. The row driver of claim 5, wherein the boosted voltage comprises a reset enable signal.

9. The row driver of claim 5, wherein the select voltage comprises Vdd.

10. The row driver of claim 5, wherein the select voltage is about 3.3 volts and the boosted voltage is about 4.2 volts.

11. The row driver of claim 5, wherein the transistor comprises a PMOS transistor including a source connected to the first line and an n-well connected to the second line.

12. The row driver of claim 6, wherein the second circuit is coupled to a bus of another row driver.

13. The row driver of claim 12, wherein the second circuit is operative to couple to the second line to the bus in response to a select signal on the bus of said another row driver.

14. The row driver of claim 6, wherein the second circuit comprises a plurality of PMOS transistors, each

PMOS transistor including a source and an n-well coupled to the second line.

15. The row driver of claim 5, wherein the bus comprises a shared row-reset bus.

16. A sensor comprising:

a pixel array including a plurality of pixels arranged in rows and columns;

a plurality of buses, each bus coupled to pixels in one row of the pixel array;

a first line operative to carry a select voltage;

a second line operative to carry a row enable voltage;

a charge pump boost circuit operative to drive the second line to a boosted voltage, said boosted voltage being higher than the select voltage;

a plurality of row drivers, each row driver coupled to an associated one of the buses and including a first circuit operative to couple said bus to the first line in response to a row select signal, said first circuit including a transistor coupled to the second line.

17. The row driver of claim 16, further comprising a second circuit operative to couple the bus to the second line in response to a row reset signal.

18. The row driver of claim 16, wherein the transistor is coupled to the second line such that there is no parasitic diode leakage between the first line and the second line through the transistor in response to the second line being driven to the boosted voltage.

19. The row driver of claim 16, wherein the boosted voltage comprises a reset enable signal.

20. The row driver of claim 16, wherein the select voltage comprises Vdd.

21. The row driver of claim 16, wherein the select voltage is about 3.3 volts and the boosted voltage is about 4.2 volts.

22. The row driver of claim 16, wherein the transistor comprises a PMOS transistor including a source connected to the first line and an n-well connected to the second line.

23. The row driver of claim 17, wherein the second circuit is coupled to a bus of another row driver.

24. The row driver of claim 23, wherein the second circuit is operative to couple to the second line to the bus in response to a select signal on the bus of said another row driver.

25. The row driver of claim 17, wherein the second circuit comprises a plurality of PMOS transistors, each PMOS transistor including a source and an n-well coupled to the second line.

26. The row driver of claim 16, wherein the bus comprises a shared row-reset bus.

27. The sensor of claim 16, wherein each pixel comprises an active pixel sensor including a photoreceptor and an in-pixel follower transistor.